REMARKS

This Amendment is submitted in response to the Office Action dated December 19, 2005, having a shortened statutory period set to expire March 19, 2006.

At page 2 of the present Office Action, Claims 1, 5-6, 8 and 11-12 are rejected under 35 U.S.C. § 112, second paragraph, as indefinite based upon a belief that it is unclear where the specification describes the structure corresponding to claim elements set forth in the means-plus-function format permitted under 35 U.S.C. § 112, sixth paragraph. In response, Applicant has amended each of the rejected claims to eliminate means-plus-function language. In addition, Applicant respectfully points out that the claimed memory controller is depicted at reference numeral 18 in Figures 1 and 9 and described in detail throughout the specification. Applicant therefore respectfully submits that the rejection under 35 U.S.C. § 112, second paragraph, is overcome.

Next, at page 3 of the present Office Action, Claims 1-17 are rejected under35 U.S.C. § 102 as unpatentable in view of U.S. Patent No. 6,697,919 to *Gharachorloo et al.* (*Gharachorloo*). That rejection is respectfully traversed, and favorable reconsideration of the claims is requested.

Applicant respectfully submits that *Gharachorloo* does not render exemplary Claim 1 unpatentable under 35 U.S.C. § 102 because that reference does not teach or suggest each claimed feature, and in particular, does not teach or suggest:

> ... wherein said memory controller, responsive to a memory access request, directs an access to a selected row among the plurality of rows in the system memory to service the memory access request and speculatively causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism.

With respect to the foregoing feature of exemplary Claim 1, page 5 of the present Office Action cites col. 7, paragraphs 1-2 of *Gharachorloo*, which generally describes the operation of

arbiter 154 of *Gharachorloo's* switch fabric 152. The cited passage does not disclose a memory controller, and in particular, does not teach or suggest a memory controller that "speculatively causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism." Consequently, Applicant respectfully submits that the rejection of exemplary Claim 1, similar Claims 8 and 13, and their respective dependent claims under 35 U.S.C. § 102 in view of *Gharachorloo* are overcome.

Applicant further submits that the rejections of Claims 3, 4, 10 and 15 are overcome because *Gharachorloo* does not teach or suggest that "said access history mechanism maintains a respective memory access history for each of a plurality of threads" as recited in Claim 3, or "on a per-bank basis," as recited in Claims 4, 10 and 15. At page 6 of the present Office Action, *Gharachorloo's* disclosure of SMT, instruction-level parallelism and out-of-order execution are relied upon as teaching the foregoing claim features. However, *Gharachorloo* does not teach or suggest that *Gharachorloo's* memory directory 180 maintains "a respective memory access history for each of a plurality of threads" or on "a per-bank basis" as required by the Examiner's rejection. Because *Gharachorloo* does not teach or suggest the features recited in Claims 3-4, 10 and 15, Applicant respectfully submits that the rejections of these claims are overcome.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447.**

Respectfully submitted,

Brian F. Russell
Registration No. 40,796
DILLON & YUDELL LLP
8911 N. Capital of Texas Hwy., Ste. 2110
Austin, Texas 78759
(512) 343-6116

ATTORNEY FOR APPLICANT